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(71) Applicant (for all designated States except US): COCHLEAR LIMITED [AU/AU]; 14 Mars Road, Lane Cove, NSW 2066 (AU).

(72) Inventor; and
(75) Inventor/Applicant (for US only): SELIGMAN, Peter [AU/AU]; 107 Fawkner Street, Essendon, VIC 3040 (AU).

(74) Agent: WATERMARK PATENT & TRADEMARK ATTORNEYS; Unit 1, The Village, Riverside Corporate Park, Hawthorn, VIC 3122 (AU).

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(54) Title: BATTERY MONITOR AND POWER DEMAND ADJUSTER
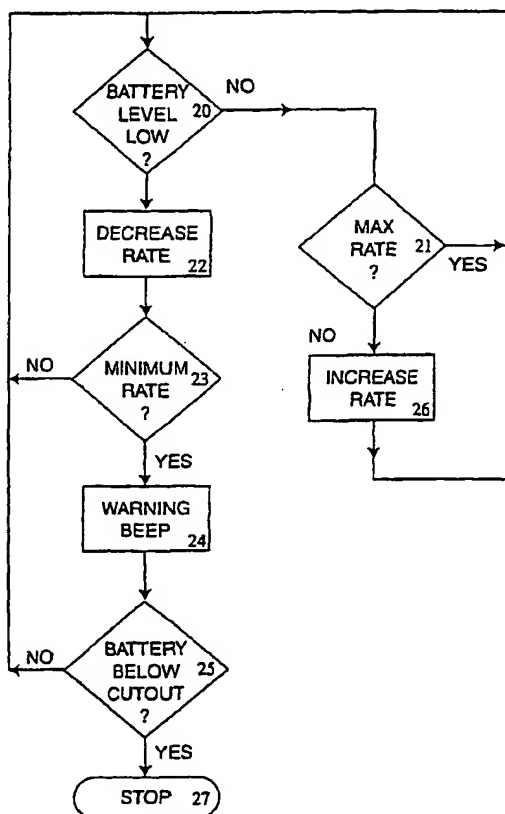
(57) Abstract: A system for monitoring and controlling power demands in devices with DC power supplies is disclosed. A device includes a control means responsive to a monitoring means. If the output voltage of the power source detected by the monitoring means falls below a first predetermined level, the power requirements of the device are reduced by the control means. If the output voltage level detected by the monitoring means falls further below a second predetermined level, the second level being lower than the first level, the control means shuts down the device. This approach has application to battery powered devices, particularly for medical applications such as cochlear implants.

BATTERY MONITOR AND POWER DEMAND ADJUSTER

Technical Field

The present invention relates generally to devices powered by energy storage arrangements, and in particular but not exclusively to prostheses and

5 stimulation devices powered by batteries.

Background Art

Many devices are powered by electrochemical cells, particularly devices for medical use. Examples of such devices include hearing prostheses, neural stimulators, pacers, drug pumps and other devices.

10 Increasingly, these devices use digital processing systems, rather than analog systems which were the standard prior art technique. One feature of digital systems is that the processor used will generally require a certain minimum voltage to operate effectively. If this is not present, the device will fail erratically. To avoid this, a system shutdown voltage level is generally used, at

15 which level the device shuts itself down. This level is often set well above the actual minimum level, to avoid the possibility of error from a dubious power supply. In contrast, prior art analog systems generally fail gradually, with progressively less performance delivered as less voltage is available from the battery. Accordingly, the user has generally more warning of impending device

20 failure.

To take the example of cochlear implants, modern speech processors are controlled by and process speech using a microprocessor. The speech processor also provides power to an induction loop, which via an inductive coupling supplies power and data to an implanted receiver stimulator unit.

25 Although in principle any suitable battery could be used to provide power to such systems, the zinc-air cell is the preferred power source. Such cells are also commonly used for applications such as external hearing aids.

Zinc air cells have several practical advantages. They have a very high energy density, and so can supply a device's requirements for a relatively long

30 period of time relative to their size and weight. They also have a relatively constant power output through most of their life, so that there is little risk of dangerous rapid discharge, for example by shorting. However, if they experience a heavy load, then it is common for the voltage to temporarily sag.

Conventionally, such devices have employed a battery monitor arrangement, whereby the voltage is monitored and if it falls below a certain level, the device is shut down. Such voltage levels are often set at a value which corresponds to a relatively high power demand, so as to prevent

5   anomalous operation due to under voltage. As a result, if even a relatively new battery is subjected to adverse conditions, for example a period of heavy load, the cell voltage may fall below the pre-defined cut-off level and the processor will be shut down. In the field of Cochlear implants such an event is inconvenient and has potentially serious implications. After shut-down, the

10   user must reset the speech processor by re-starting it, and hence the user is disconnected for a time from their hearing environment. Similar problems can arise with other battery powered digital systems, where short term conditions cause a temporary reduction in the voltage of the power supply.

It is an object of the present invention to provide an improved battery

15   monitoring arrangement in order to improve the performance of battery powered devices.

Summary of the Invention

The present invention provides, broadly, for a device in which battery performance is monitored, and in which the power demands of a device are

20   reduced to match the available battery power. This allows for what may be called graceful failure, rather than complete shut-down at an arbitrary level.

In the case of a cochlear implant, one implementation is to introduce a series of battery voltage trigger levels, at or below which levels aspects of processor performance are downgraded. A preferred implementation

25   progressively reduces the stimulation rate as the battery voltage declines, until it ultimately reaches a shut-down level. However, if the battery voltage increases before shut-down level is achieved, the stimulation rate is progressively increased to normal levels. This allows the device to cope with a degree of voltage sag without ceasing to function.

30   Alternative responses to a reduction in voltage for a cochlear implant implementation may include a change in the speech processing strategy , or other changes to reduce power requirements. In other devices, the performance of the device may be reduced by changes in the operation of

processors or other elements, without shutting down the system. These alternatives may be used separately or in combination.

Whilst the present invention has particular advantages for zinc-air cells, the principle has application to other battery-powered digital devices, 5 especially devices whose continued function, even at a reduced level of performance, is important.

Brief Description of Drawings

An implementation of the present invention will now be described with reference to the accompanying figures, in which:

10 Figure 1 is a schematic illustration of a conventional intra-cochlear implant system;

Figure 2 is a flow chart illustrating the operation of the inventive system; and

Figure 3 is a schematic diagram of a central circuit utilising the present 15 invention.

Description

The present invention will be described with particular reference to a speech processor unit for a cochlear implant system. However, it will be appreciated that the present invention has application to other devices using a 20 battery to power a digital device, with modifications appropriate to the application as would be apparent to those skilled in the art. The implementation is intended to illustrate the invention's application to a particular situation, being a speech processor for an intracochlear implant.

Referring to figure 1, a typical cochlear implant device is shown. It will 25 be appreciated that such an arrangement is well known in the art, and that the illustration and the following discussion are intended purely to provide a context for the present invention. From this figure can be seen the external component, including a speech processor 1, and an internal component including an implanted receiver and stimulator unit 6. The external component 30 further includes a microphone 2 which is shown integral with the speech processor 1. The speech processor is in this illustration constructed and arranged so that it can fit behind the outer ear 11. Alternative versions may be

worn on the body. Attached to speech processor 1 is a transmitter coil 3 which transmits the electrical signals to the implanted unit 6 via an RF link 4.

The implanted component includes a receiver coil 5 for receiving power and data from coil 3. A cable 7 extends from the implanted device 6 to the
5 cochlea 12 and terminates in an electrode array 10. The signals thus received are applied by the array 10 to the basilar membrane 8 thereby stimulating the auditory nerve 9. The operation of the device shown in figure 1 is described, for example, in the applicant's US patent No. 4532930, the disclosure fo which is hereby incorporated by reference.
10 Thus, the RF link, which is in turn powered by the speech processor 1, provides power and data to the implanted device 6. The speech processor also processes sound signals received by microphone 2, so as to send appropriate instructions for stimulation to the implanted device 6. The precise details of speech processing are not necessary for an understanding of the
15 present invention, and the skilled worker in the art will be aware that many such schemes have been used and proposed. What is pertinent is that some of these schemes, and their modes of operation, consume variable levels of power. For example, a higher rate of stimulation using a given processing scheme will generally consume more power.
20 A cochlear implant device such as that illustrated in figure 1 may be powered by zinc-air cells. Conventionally, zinc-air cells are used to power speech processor units, especially behind the ear type processors. The technology of these cells is such that even though the cell capacity is very high, only a limited current is available.
25 In existing devices, a battery monitor arrangement is provided in the speech processor 1. The monitor measures the output voltage from the battery, and if the voltage falls below a certain level, the monitor sends a signal to the processor which shuts down the processor. Thus a combination of adverse factors can cause the cell voltage to drop, causing the low voltage
30 trip to operate, switching the processor off. This may happen even if the cells are new, causing unnecessary inconvenience to the patient.

According to the present invention, this problem can be overcome by reducing the power requirements of the system when the voltage drops a

certain level. One way to reduce power requirements is to lower the stimulation rate being applied by the implant. Effectively power consumption is proportional to rate (apart from a small quiescent current). Although stimulation rate can have an effect on patient speech recognition

5   performance, it is likely that the circumstances leading to such a rate reduction are situations of severe background noise such as a noisy train. When the adverse situation has passed, the rate returns to the normal programmed rate.

According to one implementation of the present invention, the stimulation rate is modulated at a rate determined by the cell voltage. When

10   the cell voltage is above a predetermined threshold level the stimulation rate is at a pre-set normal value. When the cell voltage falls below a second predetermined threshold level, the low-voltage alarm is triggered and the speech processor shuts down in the same fashion as a prior art speech processor.

15   The cell voltage may be determined by various mechanisms. An analog or digital voltmeter device could be used, a software function within the processor, or simply an analog circuit arrangement responsive to certain voltage levels. Any suitable means may be used, as would be understood by those skilled in the art.

20   The two thresholds create an intermediate range of cell voltages within which the cell or cells are still capable of supporting some functionality, but not the full operational mode. Within this range the speech processor enters a reduced functionality mode. In one embodiment this would involve the speech processor switching to a low-power mode. It is preferable, however, that the

25   speech processor operate at a stimulation rate which is determined by the measured cell voltage, as shown in figure 2.

Referring to figure 2, a flowchart illustrating one implementation of the invention is shown. At box 20, the process determines if the battery voltage level is low, that is, below a first predetermined value. If it is, then the

30   stimulation rate is decreased at box 22. If the value at box 20 is not below a first predetermined value, then box 21 determines if the processor is operating at its maximum stimulation rate. If it is, then the process loops back to box 20.

If the rate is not at maximum, the rate is increased by a predetermined amount and the process again loops back to box 20.

If the stimulation rate has been decreased at box 22, box 23 determines if the stimulation rate is at the preset minimum rate − in other words, if it is at the minimum tolerable stimulation rate. If not, then the process loops back to box 20. If it is at minimum rate, box 24 instructs a warning beep to be provided to the user, so that the user is aware that the processor may be shut down shortly. Box 25 then tests if the battery level is below a second predetermined threshold level. If it is, then the processor is stopped at box 27 and the speech processor shuts down. If it is not at the cutoff level, the process loops back to box 20.

It will be appreciated that alternative responses to progressively lower levels could be readily implemented in a speech processor. One alternative would be to switch at a certain level to an alternative speech processing strategy, which requires less power, or provides better speech percepts at low stimulation rates. For example, at a first predetermined level the very low battery response may be to switch to another processing strategy, which copes better with progressive stimulation rate reduction than the normal strategy. Another option, for example in a processor which uses a selection of channels from a filter arrangement as a basis for stimulation, may be to reduce the number of channels processed by the filter and / or to reduce the number of channels selected as the basis for stimulation. Other alternative strategies could be used to reduce power requirements in different applications, as would be apparent to those skilled in the art. Combinations of these approaches could be used.

Preferably the method is implemented as a closed loop method. If the voltage drops below the higher threshold, the rate begins to slow gradually by introducing an additional wait period at the end of a count which determines the stimulation rate. If the voltage rises again, the wait is gradually reduced. As a result, the processor stimulates at a rate which keeps the cell voltage at close to the higher threshold. If the load increases or the cell output decreases, the rate lowers further until it is unable to keep the cell voltage at

the high threshold. The result is that the voltage continues to drop until the low threshold is reached. As this point the processor cuts out.

The stimulation rate could be determined by a measure of cell voltage which incorporates some time information. This could be, for example, the
5   average cell voltage over the last 5 minutes.

Figure 3 illustrates a practical implementation of the present invention for a cochlear implant. The illustrated system is a start pulse generator 30, which generates pulses for commencing each cycle of stimulation generation by the speech processor. The pulse rate is set by a
10   counter 32 which counts 6.4 μs ticks received on line 41. The count is set by register SPCNT 36. At count 0 the counter 32 is automatically reloaded by the output of adder 35. Input to adder 35 is the SPCNT word from register 36, and the output from a 7 bit pseudo random generator 39 with bits masked by WeightMux 38 as indicated by the weight register 40.

15   In order to provide the features of the present invention, the low battery warning operation is altered so that when the threshold is encountered the start pulse counter is increased. The wait is increased by modifying the top 3 bits of the 7 bit WEIGHT register 40 with a count from a 3 bit SLOWDOWN counter 41 . The output of this result 37 is added to SPCNT 36 to provide the
20   input to counter 32.

The SLOWDOWN counter 41 operates on the detection of the Batwarn signal from box 31.   This is when the battery voltage drops below a first predetermined level, the Batwarn setting.   When the battery voltage has dropped below this level, the SLOWDOWN counter is clocked up at the rate of
25   9.5 Hz.   If the battery voltage is above the Batwarn level, the counter is clocked down at 9.5 Hz. At each end of its range, the counter is prevented from overflowing by box 42. By this means, the period of START PULSE (SP) is increased slowly by 16* 6.4 = 102.4 μs steps from a minimum of 0 to a maximum of 7* 102.4 = 716.8 μs in addition to the value set. Assuming that
30   the SP rate is typically set to 1500 Hz, i.e. with a period of 667 μs, this means that as the battery voltage sinks below the Batwarn level, the pulse rate is gradually slowed down to approximately half of its normal rate. If the power

demands lessen, the rate will increase again to the normal rate of the start pulse counter.

Jitter in the start pulses can be used in the lower 4 or 5 bits. If 5 bits of jitter are used, the period will be for example $567 - 767 \mu s$ for no slow down,

5 then a bit D4 is over-ridden by the SLOWDOWN counter, the jitter will be 667 $- 767 \mu s$. When bit D5 is set by the counter, the jitter will be $767 - 967 \mu s$ etc. If 4 bits of jitter are used, the sequence will be 667, 769, 871 μs +/-51μs. In this way the range of jitter is reduced under some circumstances but there is a gradual progression in the overall rate change.

10 To give the patient a warning of low battery, a beep is generated when the SLOWDOWN counter first reaches its maximum count

It will be understood that the above example is merely one embodiment of the present invention, and that variations and additions are possible within

15 the broad scope of the inventive concept, as will be apparent to those skilled in the art.

CLAIMS:

1. A device powered by a DC power source, said power source being
subject to variations in voltage, said device including monitoring means for
measuring the output voltage of said power source,

    characterised in that said device includes control means responsive to
said monitoring means, said control means being operatively enabled to
reduce the power demands of said device, said control means being arranged
so that if the output voltage level detected by said monitoring means falls
below a first predetermined level, the power requirements of the device are
reduced by said control means, and that if the output voltage level detected by
said monitoring means falls below a second predetermined level, said second
level being lower than said first level, said control means shuts down the
device.

2. A device according to claim 1, wherein if the monitoring means detects
output voltage having a value between said first and second
predetermined levels, said control means is adapted to progressively
reduce the power demands of said device in accordance with a
predetermined instruction set responsive to the voltage level detected
by the monitoring means.

3. A device according to claim 3, wherein said device is controlled
digitally.

4. A device according to claim 4, wherein if said control means has
reduced the power demands of said device, and said control means
determines that the output voltage has increased, then the control
means progressively increases the power requirements of the device,
so that in one or more stages the device is restored to its normal
operating mode.

5.   A speech processor for a cochlear prosthesis, said processor being powered by a DC power source and including monitoring means for measuring the output voltage of said power source, said processor being arranged to implement speech processing strategies and stimulation strategies , and to permit one or more of the speech processing strategy, the stimulation strategy, and the stimulation rate to be changed,

characterised in that said processor includes control means responsive to said monitoring means, said control means being operatively enabled to alter one or more of the speech processing, stimulation strategy and stimulation rate implemented by said processor, said control means being arranged so that if the output voltage level detected by said monitoring means falls below a first predetermined level, the power requirements of the device are reduced by said control means altering one or more of the speech processing strategy, stimulation strategy and stimulation rate implemented by said processor, and that if the output voltage level detected by said monitoring means falls below a second predetermined level, said second level being lower than said first level, said control means shuts down the processor.

6.   A speech processor according to claim 5, wherein said control means altering one or more of the speech processing strategy, stimulation strategy and stimulation rate implemented by said processor includes one or more of reducing the stimulation rate, reducing the number of sound channels processed, and selecting an alternative speech processing   strategy.

7.   A speech processor according to claim 6, wherein if the monitoring means detects output voltage having a value between said first and second predetermined levels, said control means is adapted to progressively reduce the power demands of said device in accordance with a predetermined instruction set responsive to the voltage level detected by the monitoring means by further altering one or more of the speech processing strategy, the stimulation strategy and the stimulation rate implemented by said processor.

8.   A speech processor according to claim 5 or 6, wherein if said control means has reduced the power demands of said device, and said monitoring means determines that the output voltage has increased, then the control means progressively increases the power requirements of the device, so that in one or more stages the device is restored to its normal operating mode.

9.   A speech processor according to claim 5, wherein if the output voltage falls below said first predetermined level, the stimulation rate of said processor is reduced gradually to a predefined minimum level, and if said output voltage increases, the stimulation rate is gradually increased.

10.   A method of operating a device powered by a DC power source, said power source being subject to variations in voltage, said device including monitoring means for measuring the output voltage of said power source, and control means responsive to said monitoring means, said method including the steps of:

Measuring the output voltage of said power source;

If said measured output voltage falls below a first predetermined voltage level, then said control means reduces the power demands of said device; and

If said measured output voltage falls below a second predetermined voltage level, then said control means shuts down said device.

11.   A method according to claim 9, wherein said method includes the further step of:

If said measured output voltage falls between said first and second predetermined levels, then in accordance with a predetermined instruction set responsive to the voltage level

detected by the monitoring means, said control means progressively reduces the power demands of said device.

12.   A method according to claim 9 or 10, wherein said method includes the further step of:

If said control means determines that the measured output voltage has increased, then the control means progressively increases the power demands of the device, so that in one or more stages the device is restored to its normal operating mode.

13.   A method of operating a speech processor for a cochlear prosthesis, said processor being powered by a DC power source and including monitoring means for measuring the output voltage of said power source, said processor being arranged to implement speech processing strategies and stimulation strategies , and to permit one or more of the speech processing strategy, the stimulation strategy, and the stimulation rate to be changed, said processor further includes control means responsive to said monitoring means, said method including the steps of:

Measuring the output voltage of said power source;

If said measured output voltage falls below a first predetermined voltage level, then said control means reduces the power demands of said device by altering one or more of the speech processing strategy, stimulation strategy and stimulation rate implemented by said processor; and

If said measured output voltage falls below a second predetermined voltage level, said second level being lower than said first level, said control means shuts down the processor.

14.   The method according to claim 13, wherein said step of altering one or more of the speech processing strategy, stimulation strategy and stimulation rate implemented by said processor includes one or more of reducing the stimulation rate, reducing the number of sound channels processed, and selecting an alternative speech processing

strategy.

15.   The method according to claim 13, wherein said method includes the further step of:

If said measured output voltage falls between said first and second predetermined levels, then in accordance with a predetermined instruction set responsive to the voltage level detected by the monitoring means, said control means progressively reduces the power demands of said device by further altering one or more of the speech processing strategy, the stimulation strategy and the stimulation rate implemented by said processor.

16.   The method according to claim 15, wherein said method includes the further step of:

If said control means has reduced the power demands of said device, and said monitoring means determines that the output voltage has increased, then the control means progressively increases the power demands of the device, so that in one or more stages the device is restored to its normal operating   mode.

17.   The method according to claim 13, wherein if the output voltage falls below said first predetermined level, the stimulation rate of said processor is reduced gradually to a predefined minimum level, and further including the step that

If said output voltage increases, the stimulation rate is gradually increased.

Fig 1.
Prior Art

●

●

Fig 2.

3/3

Fig 3.

42
┌─────────────────────┐
│ UNDER/OVERFLOW   │
│ LIMIT   │
└─────────────────────┘

Symbolic   31
Representation
┌ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐   41
│ Vbatt ──────┐ −   │   ┌─────────────────────┐
│   ▷──────┼───▶│   SLOW DOWN   │◀── 9.5 kHz
│ Vbattwarm ──┘ +   │   │ U/D   3 BIT UP/DOWN │
└ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘   │   COUNTER   │
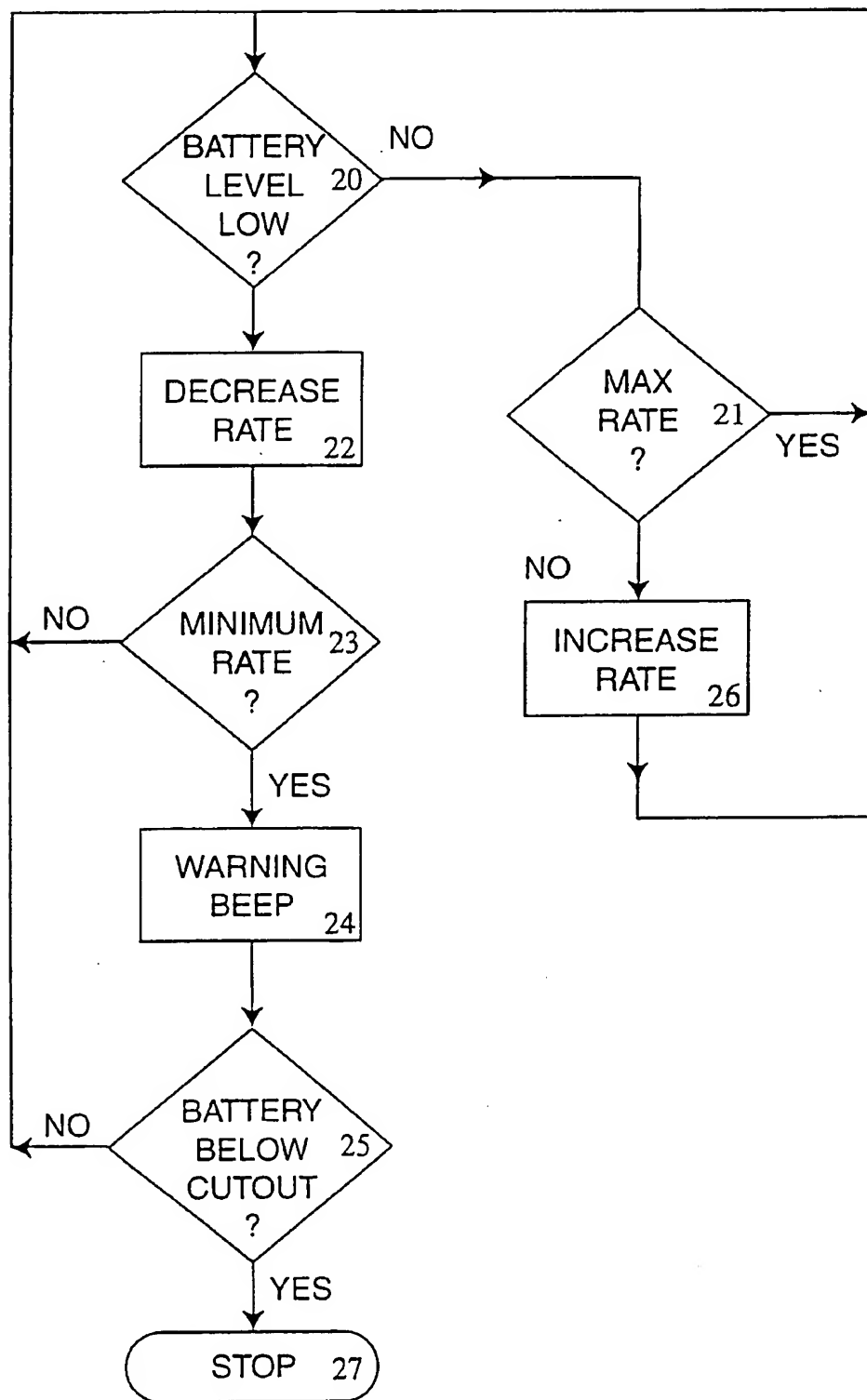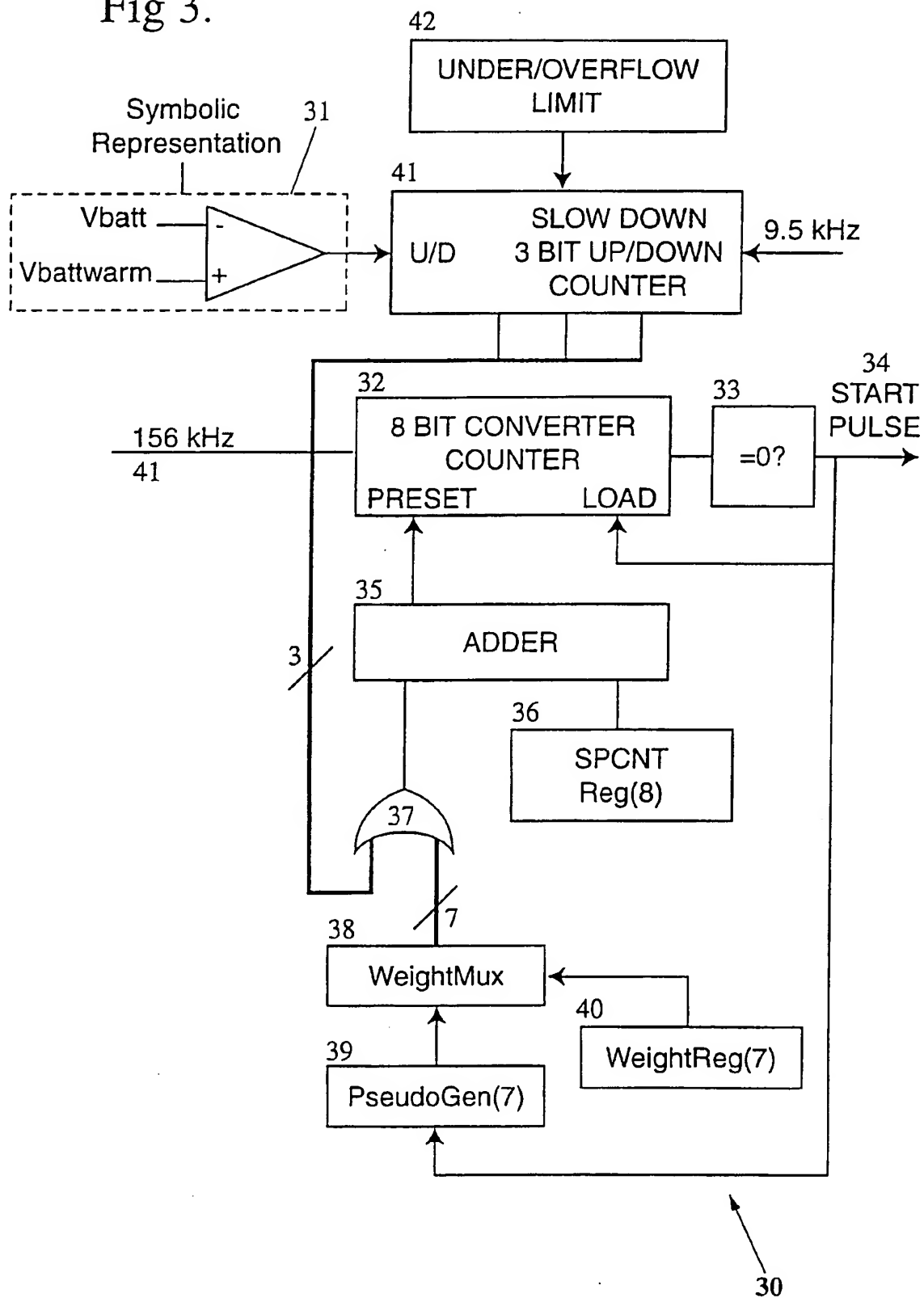   └─────────────────────┘

                          32   33   34
                          ┌─────────────────────┐   START
156 kHz   │   8 BIT CONVERTER   │ ┌─────┐ PULSE
───────────────────────── │   COUNTER   │──│ =0? │──────▶
41   │   │ └─────┘
                          │ PRESET   LOAD   │
                          └─────────────────────┘

               35
          ┌─────────────────────┐
    3 /   │   ADDER   │
          └─────────────────────┘
                               36
                          ┌──────────┐
                          │ SPCNT   │
                          │ Reg(8) │
                          └──────────┘
            37

       38
  ┌──────────────┐
  │ WeightMux   │◀────────┐
  └──────────────┘   │
                        40 │
       39   ┌───────────────┐
  ┌──────────────┐   │ WeightReg(7) │
  │ PseudoGen(7) │   └───────────────┘
  └──────────────┘

                                          30
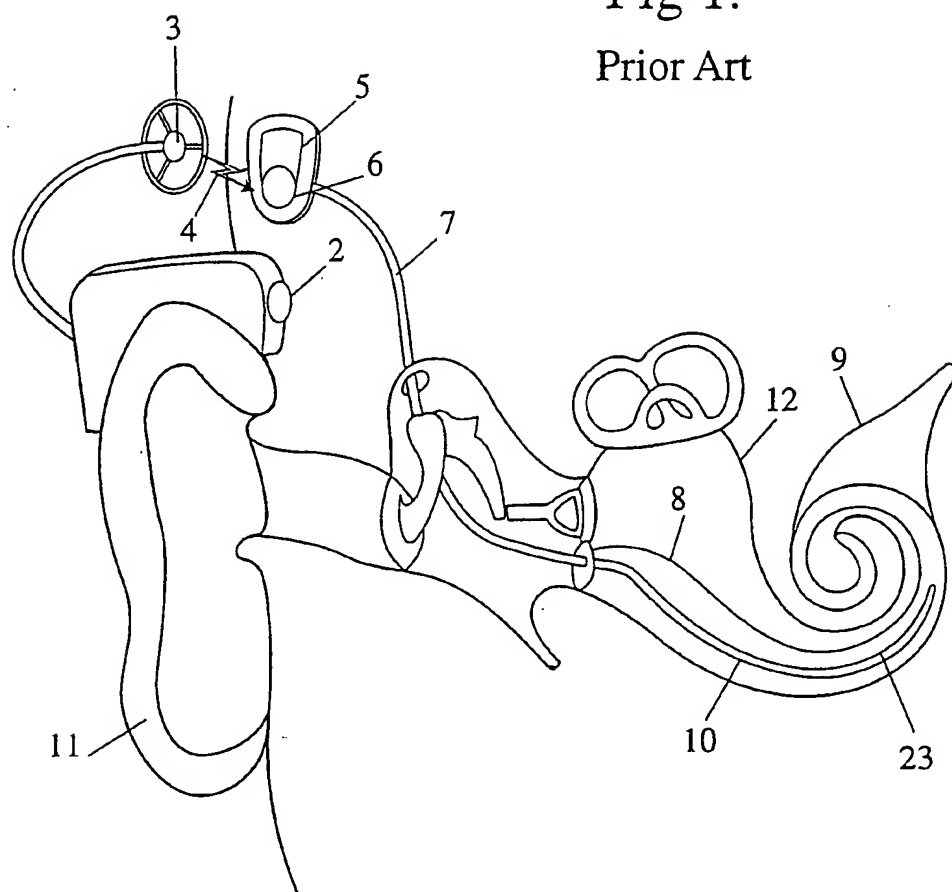
INTERNATIONAL SEARCH REPORT

A.	CLASSIFICATION OF SUBJECT MATTER

Int Cl^7:   H04R 25/00, H02J 7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B.	FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC:G01R, H01M, H02J, H04R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT: output voltage/level, battery, DC power source/supply, measure, monitor, control, load, demand, power, predetermined, threshold.

C.	DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 773 961A (CAMERON et al), 30 June 1998 Whole document Whole document	1,10 2-9, 11-17
Y	Derment Abstract Accession No. 98-304706/27, class X16, JP10108387A (KYOCERA Corp), 24 April 1998 Abstract	1,10
Y	EP 653826A (NEC Corporation), 17 May 1995 Whole Document	1,10
A	US 5 869 970A (PALM et al), 9 February 1999 Whole document	1,10

[X]	Further documents are listed in the continuation of Box C	[X]	See patent family annex

*   Special categories of cited documents:

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"X"   document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y"   document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"   document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 June 2000	2 6 JUN 2000

Name and mailing address of the ISA/AU	Authorized officer
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication. where appropriate, of the relevant passages	Relevant to claim No.
A	Derwent Abstract Accession No. 98 - 304704/27, class X12 X16, JP 10108385A (KYOCERA CORP), 24 April 1998 Abstract	1,10
A	US 5 668 465A (MAY). 16 September 1997 Whole document	1,10
A	Derwent Abstract Accession No. 94-245158/30, class S01 JP 06178456A (HITACHI KOKI KK),.26 June 1994 Abstract	1,10

INTERNATIONAL SEARCH REPORT

nformation on patent family members

.his Annex lists the known "A" publication level patent family members relating to the patent documents cited in the .bove-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which .re merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member	
US	5773961	US	5889388
EP	653826	AU	78904/94
		CA	2135963
		JP	7143673
		JP	7141072
US	5869970	US	5959371
US	5668465	NONE	

END OF ANNEX